Patent claims

1. Receiver arrangement for receiving frequency-modulated radio signals, having

- a demodulator circuit arrangement (18), which converts an intermediate-frequency signal into a voltage signal, which is applied to an input stage (22) of a signal-processing circuit arrangement (23),
- a clock-signal oscillator (26), which supplies a clock signal for the clock control of elements of the circuit arrangement,
- a test-signal generator stage (28), the input of which is connected to an output of the clock-signal oscillator (26) supplying the clock signal and the output of which is connected to an input stage (19) of the demodulator circuit arrangement (18), and
- a control circuit arrangement (12) for setting and/or testing the demodulator circuit arrangement (18), which controls the test-signal generator stage (28) for carrying out setting or testing operation and, during the setting or testing operation, sets the demodulator circuit arrangement (18) on the basis of its output signal or supplies a test-result signal indicating serviceability.

2. Receiver arrangement according to Claim 1, characterized in that the test-signal generator stage (28) is connected to the clock-signal oscillator (26), the clock signal of which serves for generating a frequency signal for reducing the frequency of a received signal to the intermediate frequency.

3. Receiver arrangement according to Claim 1 or 2, characterized in that the test-signal generator stage (28) comprises a frequency divider (30), which supplies as the output signal a frequency signal which contains a harmonic with a first frequency equal or virtually equal to the intermediate frequency.

4. Receiver arrangement according to Claim 3, characterized in that the test-signal generator stage (28) has a further frequency divider (32), the frequency

divider ratio of which is different from that of the first frequency divider (30) and the output signal of which is applied to a mixer (34), to which the output signal of the first frequency divider (30) is also fed in order to obtain a test signal which contains a different harmonic with a second frequency close to the intermediate frequency.

5. Receiver arrangement according to Claim 3 or 4, characterized in that the clock signal output of the clock-signal oscillator (26) is applied to the frequency dividers (30, 32) via in each case one of the switches (29, 33) which can be controlled by the control circuit arrangement.

6. Receiver arrangement according to one of the preceding claims, characterized in that the demodulator circuit arrangement (18) has as the input stage a bandpass filter (19), and in that the fundamental frequency of the test signal is greater than the bandwidth of the bandpass filter (19), preferably greater than twice the bandwidth, in particular greater than four times the bandwidth of the bandpass filter (19).

7. Receiver arrangement according to one of the preceding claims, characterized in that the demodulator circuit arrangement (18) has as the output stage an offset stage (21), which is connected to a voltage signal output of a demodulator circuit (20) of the demodulator circuit arrangement (18) in order to adapt the output signal of the demodulator circuit arrangement (18) to the input stage (22) of the signal-processing circuit arrangement (23).

8. Receiver arrangement according to Claim 7, characterized in that the offset stage (21) adds a direct voltage component to the voltage signal supplied by the demodulator circuit (20).

9. Receiver arrangement according to Claim 7 or 8, characterized in that the offset stage (21) is set by the control circuit arrangement (12) during setting operation on the basis of its output signal.

10. Receiver arrangement according to Claim 7 or 8, characterized in that the control circuit arrangement (12) is assigned a memory (31) in which a value for a direct voltage offset to be set, determined during the setting operation on the basis of the output signal of the offset stage (21), is stored, and in that the offset stage (21) can be set by the control circuit arrangement (12) to correspond to the stored value.

11. Method of adapting a receiving branch of a receiver arrangement, which comprises a demodulator circuit arrangement (18) converting an intermediate-frequency signal into a voltage signal, to an input stage (22) of a signal-processing circuit arrangement (23), in which

- a test signal with a known frequency is formed from a clock signal supplied by the clock-signal oscillator (26) and is applied to an input of the demodulator circuit arrangement (18), and
- the demodulator circuit arrangement (18) is set on the basis of its output signal to adapt its output signal to the input stage (22) of the signal-processing circuit arrangement (23).

12. Method according to Claim 11, characterized in that

- the test signal is formed from the clock signal supplied by the clock-signal oscillator (26) by frequency division with wave shaping, so that the test signal contains a harmonic with a first frequency equal or virtually equal to the intermediate frequency, and
- the harmonic with the first frequency is fed to a demodulator circuit (20) of the demodulator circuit arrangement (18) via a filter, preferably via a bandpass filter (19).

13. Method according to Claim 12, characterized in that a second test signal is generated by mixing the first test signal with a signal formed from the clock signal supplied by the clock-signal oscillator (26) by frequency division by a different divider factor, the frequency of which signal is equal or virtually equal to

twice the difference between the frequency of the harmonic with the first frequency and the intermediate frequency, so that the second test signal contains a harmonic with a second frequency virtually equal to the intermediate frequency.

14. Method according to Claim 13, characterized in that the first test signal and the second test signal are applied one after the other to the demodulator circuit arrangement (18), in order to determine a direct voltage offset for the adaptation of the output signal of the demodulator circuit arrangement (18) to the input stage (22) of the signal-processing circuit arrangement (23).

15. Self-testing method for testing a receiving branch of a receiver arrangement with a clock-signal generator, which has a demodulator circuit arrangement (18) converting an intermediate-frequency signal, in which

- a test signal with a known frequency is formed from a clock signal supplied by the clock-signal oscillator (26) and is applied to an input of the demodulator circuit arrangement (18), and
- a test-result signal indicating the serviceability of the receiving branch (10) is generated on the basis of the output signal of the said receiving branch.

16. Method according to Claim 15, characterized in that

- the test signal is formed from the clock signal supplied by the clock-signal oscillator (26) by frequency division with square-wave shaping, so that the test signal contains a harmonic with a first frequency equal or virtually equal to the intermediate frequency.